WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit system having a plurality of chips and making said plurality of chips transmit and receive signals to and from each other, comprising:

a bus selector device connected to said plurality of chips via a plurality of buses,

said bus selector device receiving connection information among said plurality of chips and selecting among connections of said plurality of buses in accordance with the connection information.

2. The semiconductor integrated circuit system of claim 1, wherein said bus selector device comprises:

switch means for switching among the connections of said plurality of buses; and

determination means for determining the connection information among said plurality of chips received, and for outputting a switch signal in accordance with determination results to said switch means.

3. The semiconductor integrated circuit system of claim 1, wherein said bus selector device comprises:

latch means for holding signals to be transmitted to or received from said plurality of chips to adjust timings of signal transmission and reception.

4. The semiconductor integrated circuit system of claim 1, wherein said plurality of chips include at least one master chip and a plurality of slave chips.

5. The semiconductor integrated circuit system of claim 4, wherein

said master chip outputs the connection information among said plurality of chips to said bus selector device; and

said master chip and said bus selector device are connected to each other with a single bus, said single bus carrying the connection information among said plurality of chips.

6. The semiconductor integrated circuit system of claim 4, wherein

said master chip outputs the connection information among said plurality of chips to said bus selector device; and

said master chip and said bus selector device are connected to each other with two or more buses, one of said two or more buses carrying the connection information among said plurality of chips.

7. The semiconductor integrated circuit system of claim 6, wherein

said two or more buses include a command bus, said command

bus being also used as a connection information bus to carry the connection information among said plurality of chips.

8. The semiconductor integrated circuit system of claim 6, wherein

said one of said two or more buses to carry the connection information among said plurality of chips is a specifically designed connection information bus.

9. The semiconductor integrated circuit system of claim 1, wherein the connection information among said plurality of chips is composed of a packet.

10. A semiconductor integrated circuit system having at least a master chip and a plurality of slave chips, comprising:

a bus selector device which is connected to said master chip and said plurality of slave chips with a plurality of buses and which selects among connections of said plurality of buses,

said bus selector device being arranged substantially at a same distance from said plurality of slave chips.

11. The semiconductor integrated circuit system of claim 10, wherein

said bus selector device is arranged substantially at a same distance from said master chip and said plurality of salve

~~chips.~~

12. The semiconductor integrated circuit system of claim 10, wherein

said plurality of slave chips are memory.

13. A bus selector device connected to a plurality of chips with a plurality of buses and selecting among connections of said plurality of buses, comprising:

switch means for switching among said connections of said plurality of buses; and

determination means for receiving and determining connection information among said plurality of chips, and for outputting a switch signal in accordance with determination ~~results to said switch means.~~

14. The bus selector device of claim 13 further comprising:

control signal input means for receiving a control signal from one of said plurality of chips for another chip; and

control signal output means for outputting said control signal to at least one of said plurality of chips through one of said plurality of buses selected by switching of said switch means.

15. The bus selector device of claim 13 further comprising:

data input means for receiving data from one of said plurality of chips; and

data output means for outputting said data to at least one of said plurality of chips through one of said plurality of buses selected by switching of said switch means.

16. The bus selector device of claim 15 further comprising:

a plurality of internal buses connected to said plurality of buses, said plurality of internal buses each being provided ~~with latch means.~~